## CLAIMS

What is claimed is:

1. A dual bit dielectric memory cell comprising:

a) a substrate comprising a source region, a drain region, and a channel region positioned there between;

b) a multilevel charge trapping dielectric positioned on the surface of the substrate; and

c) a control gate positioned on the surface of the multilevel charge trapping dielectric and positioned over the channel region; and

d) wherein the multilevel charge trapping dielectric includes:

i) a tunnel layer adjacent to the substrate of a first dielectric material;

ii) a top dielectric layer adjacent to the control gate of a second dielectric material; and

iii) a charge trapping layer positioned between the tunnel layer and the top dielectric layer and including a source charge trapping region and a drain charge trapping region separated by an isolation barrier there between.

2. The dual bit dielectric memory cell of claim 1, wherein the isolation barrier is an oxide.

3. The dual bit dielectric memory cell of claim 2, wherein charge trapping layer ranges from about 50 A to 100 A in thickness.

4. The dual bit dielectric memory cell of claim 3, wherein the source charge trapping region and the drain charge trapping region are comprised of a nitride compound.

5. The dual bit dielectric memory cell of claim 4, wherein the source charge trapping region and the drain charge trapping region comprise a material selected from

the group consisting of $Si_2N_4$ and $SiO_xN_4$.

6. The dual bit dielectric memory cell ell of claim 5, wherein each of the source charge trapping region and the drain charge trapping region have a lateral width beneath the top dielectric layer from about 300 A to 500 A.

7. The dual bit dielectric memory cell of claim 1, wherein the tunnel dielectric layer is comprised of material with a very low hydrofluoric acid etch rate.

8. The dual bit dielectric memory cell of claim 7, wherein the isolation barrier is an oxide.

9. The dual bit dielectric memory cell of claim 8, wherein charge trapping layer ranges from about 50 A to 100 A in thickness.

10. The dual bit dielectric memory cell of claim 9, wherein the source charge trapping region and the drain charge trapping region are comprised of a nitride compound.

11. The dual bit dielectric memory cell of claim 10, wherein the source charge trapping region and the drain charge trapping region comprise a material selected from the group consisting of $Si_2N_4$ and $SiO_xN_4$.

12. The dual bit dielectric memory cell of claim 11, wherein each of the source charge trapping region and the drain charge trapping region have a lateral width beneath the top dielectric layer from about 300 A to 500 A.

13. The dual bit dielectric memory cell of claim 12, wherein the top dielectric layer is comprised of material selected from the group consisting of an aluminum oxide compound, a Hafnium oxide compound, and a zirconium oxide compound.

14. The dual bit dielectric memory cell of claim 13, wherein the top dielectric layer is comprised of material selected from the group consisting of $Al_2O_3$, $HfSiO_x$, $HfO_2$, and $ZrO_2$.

15. A method of storing data in dual bit dielectric memory cell, the method comprising:

a) utilizing a source-to-drain bias in the presence of a control gate field to inject a charge into a source charge trapping region;

b) utilizing a drain-to-source bias in the presence of a control get field to inject a charge into a drain charge trapping region;

c) providing an isolation barrier between the source charge trapping region and the drain charge trapping region.

16. The method of claim 15, wherein the step of providing an isolation barrier includes providing an isolation barrier comprised of oxide.

17. The method of claim 16, wherein the step of providing an isolation barrier comprised of oxide includes providing an isolation barrier from about 50 A to 100 A in thickness, the step of utilizing a source-to-drain bias in the presence of a control gate field to inject a charge into a source charge trapping region includes injecting a charge into a source charge trapping region that is from about 50 A to 100 A in thickness, and the step of utilizing a drain-to-source bias in the presence of a control gate field to inject a charge into a drain charge trapping region includes injecting a charge into a drain charge trapping region that is from about 50 A to 100 A in thickness.

18. The method of claim 17, wherein the step of utilizing a source-to-drain bias in the presence of a control gate field to inject a charge into a source charge trapping region includes injecting a charge into a source charge trapping region comprising a nitride compound, and the step of utilizing a drain-to-source bias in the presence of a control

gate field to inject a charge into a drain charge trapping region includes injecting a charge into a drain charge trapping region comprising the nitride compound.

19. The method of claim 18, wherein the step of utilizing a source-to-drain bias in the presence of a control gate field to inject a charge into a source charge trapping region includes injecting a charge into a source charge trapping region comprising a material selected from the group consisting of $Si_2N_4$ and $SiO_xN_4$, and the step of utilizing a drain-to-source bias in the presence of a control gate field to inject a charge into a drain charge trapping region includes injecting a charge into a drain charge trapping region comprising the material.

20. The method of claim 19, wherein the step of utilizing a source-to-drain bias in the presence of a control gate field to inject a charge into a source charge trapping region includes injecting a charge into a source charge trapping region that extends beneath a control a length from about 300Å to about 500Å, and the step of utilizing a drain-to-source bias in the presence of a control gate field to inject a charge into a drain charge trapping region includes injecting a charge into a drain charge trapping region that extends beneath a control a length from about 300Å to about 500Å.

21. A method of fabricating a dual bit charge storage device on a silicon substrate, the method comprising:

a) fabricating a layered island on the surface of the substrate with an island perimeter defining a gate region, the layered island comprising a tunnel dielectric layer on the surface of the silicon on insulator wafer, an isolation barrier dielectric layer on the surface of the tunnel dielectric layer, a top dielectric layer on the surface of the isolation barrier dielectric layer, and a polysilicon gate on the surface of the top dielectric layer;

b) removing a portion of the isolation barrier dielectric layer to form an undercut region within the gate region;

c) depositing a charge trapping material within the undercut region.

22. The method of claim 21, further comprising implanting buried bit lines within the substrate on opposing sides of the layered island.

23. The method of claim 21, wherein the charge trapping material is a silicon nitride compound.

24. The method of claim 23, wherein the step of depositing a charge trapping material in the undercut region comprises:

depositing a layer of the silicon nitride compound on the surface of the wafer using a vapor deposition process;

performing an anisotropic etch to remove the layer of the silicon nitride compound from the horizontal surface.

25. The method of claim 21, wherein:

the tunnel dielectric layer comprises a material with a low hydrofluoric acid etch rate; and

the step of removing a portion of the isolation barrier dielectric layer to form an undercut region within the gate region comprised performing an isotropic etch using dilute hydrofluoric acid.

26. The method of claim 25, wherein the under cut region extends between 300A and 500A into the gate region.

27. The method of claim 21, wherein the isolation barrier dielectric comprises silicon dioxide and has a thickness of between 50A and 100A.

28. The method of claim 21, wherein the top dielectric layer is a compound with a dielectric constant greater than silicon dioxide and greater than the dielectric constant of the tunnel dielectric layer.

29. The method of claim 28, wherein the top dielectric layer is a compound selected from the group of $Al_2O_3$, $HfSiO_x$, $HfO_2$, and $ZrO_2$.

30. The method of claim 29, wherein the top dielectric layer has a thickness of between 70A and 130A.

31. A method of fabricating a dual bit charge storage device on a silicon substrate, the method comprising:

depositing a tunnel dielectric layer on the surface of the substrate;

depositing an isolation barrier dielectric layer on the surface of the tunnel dielectric layer;

depositing a top dielectric layer on the surface of the isolation barrier dielectric layer;

depositing a polysilicon gate layer on the surface of the top dielectric layer;

masking a gate pattern on the surface of the polysilicon gate layer to define a gate region and expose a non-gate region;

removing the polysilicon gate layer, the top dielectric layer, the isolation barrier dielectric layer and the tunnel dielectric layer in the non-gate region;

removing a portion of the isolation barrier dielectric layer to undercut the gate region and define undercut regions; and

depositing a charge trapping material within the undercut regions.

32. The method of claim 31, further comprising implanting buried bit lines on opposing sides of the gate region.

33. The method of claim 31, wherein the charge trapping material is a silicon nitride compound.

34. The method of claim 33, wherein the step of depositing a charge trapping

material within the undercut region comprises:

depositing a layer of the silicon nitride compound on the surface of the wafer using a vapor deposition process;

performing an anisotropic etch to remove the layer of the silicon nitride compound from horizontal surfaces.

35. The method of claim 31, wherein:

the tunnel dielectric layer comprises a material with a low hydrofluoric acid etch rate; and

the step of removing a portion of the isolation barrier dielectric layer to undercut the gate region comprises performing an isotropic etch using dilute hydrofluoric acid.

36. The method of claim 35, wherein the under cut region extends between 300A and 500A into the gate region.

37. The method of claim 31, wherein the isolation barrier dielectric comprises silicon dioxide and has a thickness of between 50A and 100A.

38. The method of claim 31, wherein the top dielectric layer is a compound with a dielectric constant greater than silicon dioxide and greater than the dielectric constant of the tunnel dielectric layer.

39. The method of claim 38, wherein the top dielectric layer is a compound selected from the group of $Al_2O_3$, $HfSiO_x$, $HfO_2$, and $ZrO_2$.

40. The method of claim 39, wherein the top dielectric layer has a thickness of between 70A and 130A.